

AYDIN ADNAN MENDERES UNIVERSITY COURSE INFORMATION FORM

Course Title	Basic Digital E	lektronik							
Course Code	ETO185		Couse Level		Short Cycle (Associate's Degree)				
ECTS Credit 2	Workload	50 (Hours)	Theory	2	Practice	0	Laboratory	0	
Objectives of the Course In this course; basic logic circuits, logic circuit simplification methods, logic circuits can be obtained, electrical equivalents can be obtained, making a solution to a given application problem, to gain the knowledge and skills to set up the necessary circuitry is aimed.									
Course Content Boolean Mathematics, Karnough Mapping, Deriving and simplifying a logic function of a problem, Problems of a problems of logic circuits, Logic functions, creating a time diagram, establishing and operating a logic circuit of a problem.									
Work Placement	N/A								
Planned Learning Activities and Teaching Methods			Explanation	on (Presenta	ition), Demons	tration, Prob	olem Solving		
Name of Lecturer(s)									

Assessment Methods and Criteria				
Method	Quantity	Percentage (%)		
Midterm Examination	1	40		
Final Examination	1	70		

Recommended or Required Reading

1 Course notes

Week	Weekly Detailed Cou	/eekly Detailed Course Contents				
1	Theoretical	Number Systems				
2	Theoretical	Number Systems				
3	Theoretical	Logic Gate Circuits				
4	Theoretical	Family of Integrated Circuits and Specifications				
5	Theoretical	Circuit drawing from Logic Functions				
6	Theoretical	Finding a drawn Circuit Logic Functions				
7	Theoretical	With Logic Electrical Circuits Between Conversions				
8	Theoretical	Boolean Algebra				
9	Theoretical	Midterm				
10	Theoretical	Karnaugh map				
11	Theoretical	Karnaugh map				
12	Theoretical	Removing and to simplify a problem of logic functions				
13	Theoretical	Removing and to simplify a problem of logic functions				
14	Theoretical	Create a Problem Time Charts				
15	Theoretical	Semester final exam				

Workload Calculation							
Activity	Quantity	Preparation		Duration		Total Workload	
Lecture - Theory	14		0	2		28	
Assignment	10		0	1		10	
Individual Work	10		0	1		10	
Midterm Examination	1		0	1		1	
Final Examination	1		0	1		1	
Total Workload (Hours) 50					50		
[Total Workload (Hours) / 25*] = ECTS					2		
*25 hour workload is accepted as 1 ECTS							

Learning Outcomes

1 Recognize number systems.



2	Knows the logic door circuits.	
3	Establish basic logic circuits	
4	Simplify logic circuits	
5	Solving logic problems and setting up and running circuits	

